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10/661,079	09/12/2003	Michael W. Morrow	ITL.1028US (P16764)	7093

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,079	MORROW, MICHAEL W.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2000*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-24 and 26-31* is/are pending in the application.

4a) Of the above claim(s) *7 and 25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-24 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-6,8-29 are presented for examination. Claims 7 have been canceled. TD on 06/02/06 has been received.

2. Claims 22-29 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relation of the feedback signal to the wireless interface.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1,8,13,14-16, 17,22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons follow.

4. As to claim 1, no practical application can be found. The step of determining whether execution of instruction may require a long latency is not useful, tangible , and concrete. It is not useful because no specific and substantial application can be found. Applicant is reminded that the focus is not on the step or feature taken to achieve a final useful, which is useful, concrete , and tangible, but rather the final result achieved which is useful, concrete, and tangible (see MPEP 21-6 2100-12-14). Similarly, the step of switching the thread presents no useful, tangible, concrete result. No substantial practical application can be found in this step except the thread

switching (see Benson, 409, U.S. at 71-72, 175 USPQ at 676-77). Similar analysis can be done to claims 8,13, and no specific and substantial application can be found in claims 8, 13.

5. Although claim 13 recites the computer readable medium storing the instructions, no substantial practical application of the instructions can be found in the claim. The body of claim 13 is directed to the "if" condition to switch the thread. It is an intended use, and no substantial practical application can be found. See also claim 15 for similar analysis.

6.

7. Furthermore, the computer readable medium is not limited to hardware embodiment (optical disk, page 12, lines 20-26), but also any type of media (page 13, lines 1-5). Therefore, any type of media is not necessarily a hardware.

8. Although claims 14,17, additionally recite the instruction decoder, it is directed to general arrangement of the parts, and no final result achieved which is useful, concrete, and tangible can be found (see MPEP 21-6 2100-12-14). Therefore, claim 14 has no substantial practical application.

9. As to claims 17,22, providing a feedback to switch the thread , and the feedback signal from a location in processor pipeline has no specific and substantial application. The function of the thread is not being recited in the claim. Therefore, just switching and the feeding back the signal presents no substantial practical application. The

processor pipeline is not a hardware because it is a pipeline, and a pipeline is an abstract idea, and because no structural element of the computer or the machine pipeline is being recited into the claim. Furthermore, claim 22 recites wireless interface, it raised a doubt what applicant is seeking for protection (see applicant' s specification pages 12,13). Wireless is clearly not hardware.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1,8, 13, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Borkenhagen et al. (6,697,935).

11. As to claims 1,8,13,17, Borkenhagen taught at least :

a) determining whether execution of an instruction of a first thread executed in a processor potentially causes a long latency (see the processor acted as if there had been a miss, latency, based on the cycle counter in col.13, lines 55-60) ; and

b) switching to a second thread based on the determination (see the change of the thread state in col.13, lines 55-60, see also the bit 5 of the thread switch control register 410 in col.14, lines 3-39), and executing one or more instructions of the second thread

in the processor, and storing a result (see thread state in col.11, lines 10-36) of the one or more instructions of the second thread in the processor (see execution of the thread instructions in col.5, lines 14-35, col.10, lines 16-32 for background).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claim 1-3,8,10,11,17, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Eickemeyer et al. (6,049,867) .

13. As to claim 1, Eickemeyer taught :

a) determining (by selection) whether execution of an instruction of a first thread may require a long latency (see the current thread compared to the thread of least likely run thread in col.6, lines 45-50)

b) switching to a second thread (e.g. the least likely run thread) based on the determination, executing the instructions of the second thread (see switched current thread which was least run), storing the results of the instructions (see the setting of states of the thread in col.6, lines 45-50)

14. See also the steps of 98 or 100 for the changing to another thread after the enablement in col.6, lines 25-50).

15. As to the applicant's newly remark that the claimed invention's directed to potential latency while Eickemeyer is directed to actual latency, examiner would like point out that Eickemeyer was also directed to potential latency (see the selection of the least likely run thread and switched to the least likely run thread from the current thread in col.6, lines 45-50).

16. For reason why memory miss caused long latency and why latency avoided, see col.6, lines 45-50, see also the thread switch due to the miss in col.7, lines 6-56.

17. As to claim 8, Eickemeyer taught switching from a first thread to a second thread if condition that may result stall of a processor pipeline occurs during execution of the first thread processor pipeline (see either the miss condition or the ready condition in fig.3 before changing to another thread or least used thread).

18. As to claims 2,10, Eickemeyer executing at least one additional instruction (see saving the state of thread I or determination of the enable thread in col.6, lines 11-36, saving and enabling were done by implicit command, or the like.) in the first thread while preparing (see determination of ready thread before changing to another thread) to switch to the second thread [another thread or ready thread or the least run thread].

19. As to claims 3,11, Eickemeyer also included a stochastic analysis (see valid mark) of whether the instruction will result a long latency.

20. As to claim 17, As to applicant's remark regarding the feedback signal generated in the second stage and the feedback loop between multiple pipeline stages to provide feedback signal, no specific type of feedback signal ahs been reflected into the claim, therefore, any signal feeding back can b e a feedback signal. Eickemeyer taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop for change to another thread in fig.4) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see YES) . The location not explicitly shown, but examiner holds Eickemeyer must have a location in his processor.

21. As to new claim 30, see selectively outputted instructions for various instruction processing units (load/store, branch etc.) in col.3, lines 40-52.

22. Claim 1-9, 11-14,16-21, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkenhagen et al. (6,076,157)

23. As to claims 1, 13, Borkenhagen taught (see fig.6) :

a) determining whether execution of an instruction of a first thread may require a long latency (see the first execution attempt of the instruction of thread T0 in 620);

b) switching to a second thread [T1] the instruction may require the long latency (see the switch to a second thread T1 upon no completion of the first instruction in 630, col.16, lines 44-47).

24. For the long latency , see cache miss required a large number of cycle to complete in col.15, lines 44-67, col.16, lines 1-31 for how the number of cycles thrashed.

25. As to applicant's remark that Borkenhagen was directed to actual inability to execute an instruction, Borkenhagen did teach the determination of whether execution of an instruction of a first thread may require a long latency (see the first execution attempt of the instruction of thread T0 in 620 in fig.6. See also attempt to switch back , or return to T0 in col.16, lines 47-65);

26. As to applicant's remark that actual failure to execute is not a potential cause of a long latency, applicant is reminded that actual failure to execute is a likely cause of a long latency.

27. As to applicant's remark that Borkenhagen's lookup table is not a lookup table to determine the potential latency, Borkenhagen taught a lookaside table that included virtual to real address mapping (see the control register bit assignment in col.13, lines 29-67, col.4, lines 1-21, see also the comparison of threshold value with the counter col.16, lines 11-37) . These entries in the lookaside table were addresses for read and write purpose. A unsuccessful lookup into the table would lead to latency in reading. Therefore, Borkenhagen's lookaside table did determine a potential latency.

28. As to claims 3,11, Borkenhagen also included a stochastic analysis (see cache miss in col.15, lines 43-61) of whether the instruction will result a long latency.

29. AS to claims 4,14, Borkenhagen also taught a lookup table (the control register bit assignment in col.13, lines 29-67, col.4, lines 1-21, see also the comparison of threshold value with the counter col.16, lines 11-37).

30. As to newly amended claim 14, no specific type of instruction decoder has been reflected into the claim. Therefore, it is read as an instruction decoder in general. The feedback has to come from instruction decoder for command purpose.

31. As to claims 5, 12, 16, 18, 19, 20, Borkenhagen also taught feedback to the fetch unit (see fetch requests for fetch in col.8, lines 50-63). No instruction decoder explicitly shown, but Borkenhagen taught the predetermined conditions for switching could done by hardware and software (see col.12, lines 38-65), therefor, it must have an instruction decoder. See also the instruction unit 220. No specific type of instruction decoder has been reflected into the claim. Therefore, it is read as an instruction decoder in general. Examiner also holds that instruction decoder in general had been known in the art.

32. As to claim 21, Borkenhagen included list of predetermined conditions (see fig.5).

33. As to claim 6, Borkenhagen also included more than ten cycles (see 30 cycles in col.6, lines 45-52).

34. As to claim 8, Borkenhagen taught a switching from a first thread to a second thread if condition that may result stall of a processor pipeline occurs during execution of the first thread processor pipeline (see the comparison of the threshold before switching thread in col.15, lines 62-67, col.16, lines 1-27) .

35. As to claim 9, Borkenhagen also taught a lookup table (the control register bit assignment in col.13, lines 29-67, col.4, lines 1-21, see also the comparison of threshold value with the counter col.16, lines 11-37).

36. As to claim 17, Borkenhagen taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop to return to thread T0 in fig.6) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see the state signals) .

37. As to applicant's remark that software feedback loop does not teach hardware feedback loop, applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite hardware feedback loop.

38. As to claim 30, see different type of instructions for VLIW and superscalar in col.3, lines 20-33. See also the thread state bits 4:7 for indicating the load instruction or store instruction in col.10, lines 42-43. The load instruction is one type and the store instruction is another type of instruction.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 2 , 10 , 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen in view of Chaudhry (2003/0018826)

40. As to claims 2,10, limitations of parent claims have been discussed above. Borkenhagen did not specifically show the executing of at least one additional instruction in the first thread while preparing to switch to the second thread . However, Chaudhry taught a system allowing continuing execution of a current thread while switching to another thread (see Paragraph [0012]). It would have been obvious to one of ordinary skill in the art to use Chaudhry in Borkenhagen for executing additional instruction while switching a second thread as claimed because the use of Chaudhry could provide Borkenhagen the ability to maintain the processing of the pending thread before the actual thread switch occurred , thereby reducing the time wasted on the switching, and because Borkenhagen also taught an evaluation of the threshold of the thread, no switch would occur if no instruction could be executed (see col.16, lines 18-25), which was a suggestion of the need for continuing the execution of the instructions in the current thread while switching the second thread in order to minimize the latency on the result of the switching , and for doing so, provide a motivation.

41. Claims 22, 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen (6,076,157) in view of Rompaey et al. (5,870,588) .

42. As to claim 22, Borkenhagen taught a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread (see the feedback loop to return to thread T0 in fig.6) , the feedback signal to originate from a location in the processor pipeline before instruction execution (for feedback signal, see the state signals) .

Borkenhagen did not specifically teach the wireless interface as claimed. However, Rompaey et al. (5,870,588) taught a wireless network of RISC related processor (see col.1, lines 18-24 for wireless products, see col.18, lines 31-46 for the RISC processor). It would have been obvious to one of ordinary skill in the art to use Rompaey in Borkenhagen for including he wireless as claimed because the use of Rompaey could expand the Borkenhagen's system capability to adapt to different type of devices, and because Borkenhagen also taught a RISC architecture for supporting unthreaded switching (see col.4, lines 46-67), which was an indication of the applicability of the wireless (taught by Rompaey) into Borkenhagen for providing high performance thread switching, for the above reasons , provided a motivation.

43. As to the newly amended feature of feedback signal generated in the instruction decoder to instruction fetch unit , Borkenhagen taught a feedback to the fetch unit (see fetch requests for fetch in col.8, lines 50-63). No instruction decoder explicitly shown. Since a fetch command (the fetch request) had to be read and understood by the system, the fetch command must be generated from an instruction decoder. In other words, without a decoding, the fetch request could not have been recognized. Since Borkenhagen taught the predetermined conditions for switching could done by hardware

and software (see col.12, lines 38-65), Borkenhagen must have an instruction decoder to generate a feedback to a fetch unit (See also the instruction unit 220).

44. As to applicant's remark that Rompaey is directed to non-analog art, examiner would like to point out that both Borkenhagen (a RISC architecture for supporting unthreaded switching , col.4, lines 46-67) and Rompaey were directed to a solution for a particular problem (see Rompaey's wireless network of RISC related processor in col.1, lines 18-24 for wireless products, see col.18, lines 31-46 for the RISC processor).

45. As to claims 25-28, Borkenhagen also taught feedback to the fetch unit (see fetch requests for fetch in col.8, lines 50-63). No instruction decoder explicitly shown, but Borkenhagen taught the predetermined conditions for switching could done by hardware and software (see col.12, lines 38-65), therefore, it must have an instruction decoder. See also the instruction unit 220.

46. As to claim 29, examiner holds that a dipole antenna had been known in the art. Since Rompaey already taught wireless network, one ordinary skill in the art should be able to recognize a dipole antenna could be applied to the wireless network.

47. Claims 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen (6,076,157) in view Rompaey (5,870,588) as applied to claim 22, and further in view of in view of Chaudhry (2003/0018826).

48. As to claims 23, Borkenhagen did not specifically show the executing of at least one additional instruction in the first thread while preparing to switch to the second thread . However, Chaudhry taught a system allowing continuing execution of a current thread while switching to another thread (see Paragraph [0012]). It would have been obvious to one of ordinary skill in the art to use Chaudhry in Borkenhagen for executing additional instruction while switching a second thread as claimed because the use of Chaudhry could provide Borkenhagen the ability to maintain the processing of the pending thread before the actual thread switch occurred , thereby reducing the time wasted on the switching, and because Borkenhagen also taught an evaluation of the threshold of the thread, no switch would occur if no instruction could be executed (see col.16, lines 18-25), which was a suggestion of the need for continuing the execution of the instructions in the current thread while switching the second thread in order to minimize the latency on the result of the switching , and for doing so, provide a motivation.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Nishiyama (6,775,740) is cited for the teaching of continuing the execution of a first thread while preparing the switching to second thread (see col.6, lines 59-67, col.7, lines 1-7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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